Amendments to the Claims

Please amend the second claim identified as claim 2 as shown below.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Original) A control signal generation circuit comprising:

an input terminal;

a first output terminal; and

a second output terminal,

wherein the control signal generation circuit receives, in response to a clock signal, an input signal inputted to the input terminal and outputs a column latch signal and a data input/output command signal, which are separately activated and have a first time interval therebetween, to the first output terminal and the second output terminal, respectively, each in response to a test enable signal at a first state, or outputs the column latch signal and the data input/output command signal, which are separately activated and have a second time interval therebetween, to the first output terminal and the second output terminal, respectively, each in response to a test enable signal at a second state,

wherein the first time interval and the second time interval are controlled in units of bit time of the clock signal, and the second time interval is controlled to be smaller than the first time interval.

2. (Original) The control signal generation circuit of claim 1, wherein the first time interval and the second time interval each amount to a time from when the column latch signal is activated to when the data input/output command signal is activated.

3 [[2]]. (Currently Amended) A control signal generation circuit comprising:

a first latch which latches an input signal in response to a clock signal;

a second latch which latches an output signal of the first latch in response to the clock signal;

a selection circuit which outputs the output signal of the first latch or an output signal of the second latch as a column latch signal in response to a test enable signal; and

a third latch which latches the output signal of the second latch as a data input/output command signal in response to the clock signal,

wherein the amount of time from when the column latch signal is activated to when the data input/output command signal is activated is controlled in units of bit time of the clock signal.

4. (Original) The control signal generation circuit of claim 3, wherein the input signal is generated by decoding a data write/read command signal and is activated in response to the data write/read command signal.

5. (Original) The control signal generation circuit of claim 3 further comprising:

a first inverter which is connected between an output terminal of the first latch and a first input terminal of the selection circuit;

a second inverter which is connected between the output terminal of the first latch and an input terminal of the second latch; and

a third inverter which is connected between the output terminal of the second latch and an input terminal of the third latch,

wherein the output terminal of the second latch is connected to a second input terminal of the selection circuit.

6. (Original) The control signal generation circuit of claim 3, wherein the output signal of the first latch is an inverted signal of the input signal.

7. (Original) A control signal generation circuit comprising:

a first latch which latches an input signal in response to a clock signal;

a second latch which latches an output signal of the first latch in response to the clock signal;

a third latch which latches an output signal of the second latch in response to the clock signal;

and

a selection circuit which outputs one of the output signal of the second latch and an output signal of the third latch in response to a test enable signal,

wherein the amount of time from when the output signal of the first latch is activated to when an output signal of the selection circuit is activated is controlled in units of bit time of the clock signal.

8. (Original) The control signal generation circuit of claim 7 comprising:

a first inverter which inverts the output signal of the first latch;

a second inverter which is connected between an output terminal of the first latch and an input terminal of the second latch; and

a third inverter which is connected between an output terminal of the second latch and an input terminal of the third latch,

wherein the selection circuit has a first input terminal connected to an output terminal of the third latch and a second input terminal connected to the output terminal of the second latch.

9. (Original) The control signal generation circuit of claim 7, wherein the output signal of the first latch is a column latch signal, and the output signal of the selection circuit is a data input/output command signal.

10. (Original) The control signal generation circuit of claim 7, wherein the output signal of the first latch is an inverted signal of the input signal.

11. (Original) A method for generating a control signal, the method comprising:

receiving a data write/read command signal inputted to an input terminal of a control signal generation circuit, in response to a clock signal; and

outputting a column latch signal and a data input/output command signal, which are separately activated and have a first time interval therebetween, to the first input terminal and the second input terminal, respectively, each in response to a test enable signal at a first state, or

outputting the column latch signal and the data input/output command signal, which are separately activated and have a second time interval therebetween, to the first output terminal and the second output terminal, respectively, each in response to a test enable signal of a second state,

wherein the first time interval and the second time interval are controlled in units of bit time of the clock signal, and the second time interval is controlled to be smaller than the first time interval.

12. (Original) The method of claim 11, wherein the first time interval and the second time interval each amount to a time from when the column latch signal is activated to when the data input/output command signal is activated.